Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original) A method of forming dual gate dielectric layers on a substrate, comprising:

(a) providing a substrate with isolation regions that separate device areas;

(b) depositing an interfacial layer on said substrate;

(c) depositing a high k dielectric stack on said interfacial layer;

(d) removing the interfacial layer and high k dielectric stack over one device area; and

(e) growing a second dielectric layer on the exposed device area, said growth simultaneously anneals said high k dielectric layer.

Claims 2 - 31 (cancelled)

Claim 32 (new) A structure that includes a MOSFET which is a low power device formed on a first device area and an adjacent MOSFET which is a high performance device formed on a second device area on a substrate, comprising:

a substrate having shallow trench isolation (STI) regions that separate a first device area from a second device area, said first and second device areas include lightly doped and heavily doped source/drain regions;

an interfacial layer having a first thickness formed on said first device area;

a high k dielectric stack having a second thickness formed on said interfacial layer;

a first gate electrode with a spacer on each of its two sides formed on said high k dielectric stack;

an ultra thin dielectric layer having a third thickness formed on said second device area; and

a second gate electrode with a spacer on each of its two sides formed on said ultra thin dielectric layer.

Claim 33 (new) The structure of claim **32** wherein the interfacial layer is comprised of silicon nitride, SiO_2, or silicon oxynitride with a thickness between 0 and about 30 Angstroms.

Claim 34 (new) The structure of claim **32** wherein the high k dielectric stack is comprised of one or more of Ta_2O_5, TiO_2, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, L_2O_3, and their aluminates and silicates.

Claim 35 (new) The structure of claim **32** wherein the thickness of the high k dielectric stack is from about 15 to 100 Angstroms.

Claim 36 (new) The structure of claim **32** wherein the first and second gate electrodes are comprised of doped or undoped polysilicon.

Claim 37 (new) The structure of claim **32** wherein the ultra thin dielectric layer is comprised of SiO_2 or silicon oxynitride with an effective oxide thickness of less than 10 Angstroms.

Claim 38 (new) The structure of claim **32** wherein the ultra thin dielectric layer is silicon oxynitride and the high k dielectric stack is comprised of ZrO_2 and Al_2O_3.

Claim 39 (new) The structure of claim **32** wherein the ultra thin dielectric layer is SiO_2 and the high k dielectric stack is comprised of HfO_2.

Claim 40 (new) The structure of claim **32** further comprised of a silicide layer formed on said substrate above said heavily doped source/drain regions and on said first and second gate electrodes.

Claim 41 (new) A structure that includes a MOSFET which is a low power device formed on a first device area, a MOSFET which is a high performance device formed on a second device area, and a MOSFET which is a I/O device formed on a third device area on a substrate, comprising:

a substrate having first, second, and third device areas and shallow trench isolation (STI) regions that separate adjacent device areas, said first, second, and third device areas include lightly doped and heavily doped source/drain regions;

an interfacial layer having a first thickness formed on said first device area;

a high k dielectric stack having a second thickness formed on said interfacial layer;

a first gate electrode with a spacer on each of its two sides formed on said high k dielectric stack;

an ultra thin dielectric layer having a third thickness formed on said second device area;

a second gate electrode with a spacer on each of its two sides formed on said ultra thin dielectric layer;

a second dielectric layer having a fourth thickness formed on said third device area; and

a third gate electrode with a spacer on each of its two sides formed on said second dielectric layer.

Claim 42 (new) The structure of claim **41** wherein the interfacial layer is comprised of silicon nitride, SiO_2, or silicon oxynitride with a thickness of between 0 and about 30 Angstroms.

Claim 43 (new) The structure of claim **41** wherein the high k dielectric stack is comprised of one or more of Ta_2O_5, TiO_2, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, L_2O_3, and their aluminates and silicates.

Claim 44 (new) The structure of claim **41** wherein the thickness of the high k dielectric stack is from about 15 to 100 Angstroms.

Claim 45 (new) The structure of claim **41** wherein said first, second, and third gate electrodes are comprised of doped or undoped polysilicon.

Claim 46 (new) The structure of claim **41** wherein the ultra thin dielectric layer is comprised of SiO_2 or silicon oxynitride with an effective oxide thickness of less than about 10 Angstroms.

Claim 47 (new) The structure of claim **41** wherein the second dielectric layer is SiO_2 with a thickness from about 10 to 100 Angstroms.

Claim 48 (new) The structure of claim **41** wherein the ultra thin dielectric layer is silicon oxynitride and the high k dielectric stack is comprised of ZrO_2 and Al_2O_3.

Claim 49 (new) The structure of claim **41** wherein the ultra thin dielectric layer is SiO_2 and the high k dielectric stack is comprised of HfO_2.

Claim 50 (new) The structure of claim **41** further comprised of a silicide layer formed on said substrate above heavily doped source/drain regions and on said first, second, and third gate electrodes.